a metallic layer formed above said dielectric layer;

means for emitting electrons through said metallic layer; and

a n+ region formed above a substrate such that said p region is formed within said n+ region.

2. The electron emitter according to claim 1, further comprising:

a substrate below said p region.

3. The electron emitter according to claim 1, wherein said p region is formed from a semiconductor.

4. The electron emitter according to claim 3, wherein said semiconductor includes at least one of Si, Ge, GaP, InP, InGaAs, and InGaP.

5. The electron emitter according to claim 3, wherein hole concentration level of said p region ranges substantially between 10^{16} and 10^{19} cm^{-3}

6. The electron emitter according to claim 1, further comprising:

a p electrode formed above and making electrical contact with said p region.

7. The electron emitter according to claim 1, further comprising:

an M electrode formed above and making electrical contact with said metallic layer.

8. The electron emitter according to claim 1, wherein an electron concentration level of said n+ region is greater than a hole concentration level of said p region.

9. The electron emitter according to claim 1, wherein said n+ region is formed from materials with wider band gap than said p region.

10. The electron emitter according to claim 1, wherein a thickness of said p region is less than a diffusion length of non-equilibrium electrons in said p region.

11. The electron emitter according to claim 1, wherein a thickness of said metallic layer is on the order of or less than a mean free path for electron energy.

12. The electron emitter according to claim 1, further comprising:

an n electrode formed above and making electrical contact with said n+ region.

13. The electron emitter according to claim 1, wherein said metallic layer 240 is formed from materials including at least one of Au, Ag, Al, Gd, W, Pt, Ir, Pd, and alloys thereof.

14. An electron emitter comprising:

a p region;

a dielectric layer formed above said p region;

a metallic layer formed above said dielectric layer;

a n+ region formed above a substrate such that said p region is formed within said n+ region; and

at least one voltage biasing source electrically connected to said p region and said metallic layer such that electrons pass through said metallic layer.

15. The electron emitter according to claim 14, wherein said at least one voltage biasing source is connected such that said electrons tunnel through said dielectric layer prior to passing to said metallic layer.

16. The electron emitter according to claim 14, further comprising at least one of:

a p electrode formed above and making electrical contact with said p region; and

an M electrode formed above and making electrical contact with said metallic layer.

17. The electron emitter according to claim 14, wherein an electron concentration level of said n+ region is greater than a hole concentration level of said p region.

18. The electron emitter according to claim 14, wherein said n+ region is formed from materials with wider band gap than said p region.

19. The electron emitter according to claim 14, wherein a thickness of said p region is less than a diffusion length of non-equilibrium electrons in said p region.

20. The electron emitter according to claim 14, further comprising:

an n electrode formed above and making electrical contact with said n+ region.

21. The electron emitter according to claim 14, wherein a thickness of said metallic layer is on the order of or less than a mean free path for electron energy.

22. The electron emitter according to claim 14, wherein a thickness of said dielectric layer is such that a dielectric breakdown field F_b of said dielectric layer substantially meets the condition $1.5 * 10^7$ V/cm $\leq F_b \leq 2 * 10^7$ V/cm.

23. The electron emitter according to claim 1, wherein a thickness of said dielectric layer is such that a dielectric breakdown field F_b of said dielectric layer substantially meets the condition $1.5 * 10^7$ V/cm $\leq F_b \leq 2 * 10^7$ V/cm.

24. An electron emitter comprising:

an n+ region;

a p region above said n+ region;

a dielectric layer formed above said p region;

a metallic layer formed above said dielectric layer;

a n+ region formed above a substrate such that said p region is formed within said n+ region; and

at least one voltage biasing source electrically connected to said n+ region and to at least one of said p region and said metallic layer such that a potential on said p region is positive relative to said n+ region.

25. An electron emitter, comprising:

an n+ region;

an n electrode in electrical contact with said n+ region;

a p region above and in contact with said n+ region;

a p electrode in electrical contact with said p region;

a dielectric layer formed above said p region;

a metallic layer formed above said dielectric layer;

an M electrode in electrical contact with said metallic layer;

a n+ region formed above a substrate such that said p region is formed within said n+ region; and

at least one voltage biasing source connected to at least one of said n, p, and M electrodes such that electrons tunnel through said dielectric layer and pass through said metallic layer.